IDEC Chip Design Contest

A High-Voltage Active Bootstrap Gate Driver Using VSW Zero Crossing Sensing and Dynamic Dead Time Control Techniques for GaN-based Automotive Electronics

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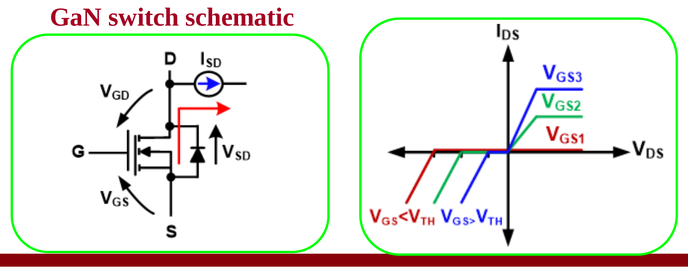
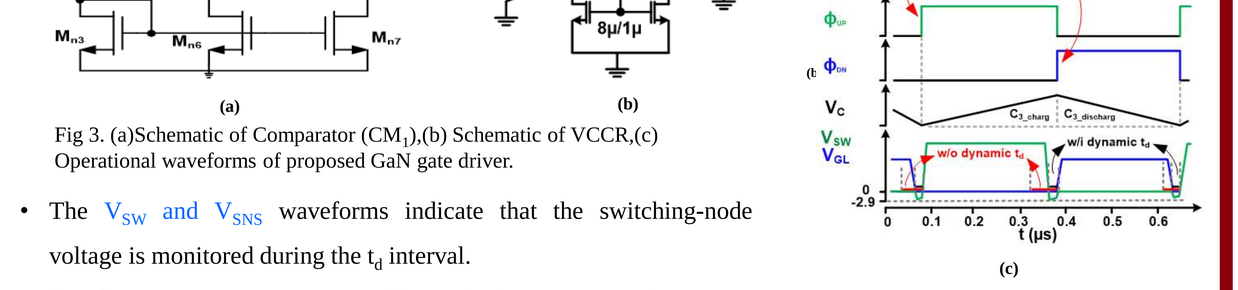
Introduction

- GaN power devices are widely used in high-frequency DC-DC converters because they provide fast switching, low loss, and high power density.
- However, GaN devices have no intrinsic body diode or PN junction.
- When V_{GS} reaches V_{TH}, the device turns on and conducts through the channel.
- In reverse-polarity conditions, GaN can still conduct current from source to drain (V_{SD}).
- This reverse conduction strongly affects switching performance in GaN converters.
- Therefore, GaN converters need careful gate driver and deadtime (t_d) design for safe and efficient operation.

GaN switch schematic



Proposed bootstrap GaN gate driver

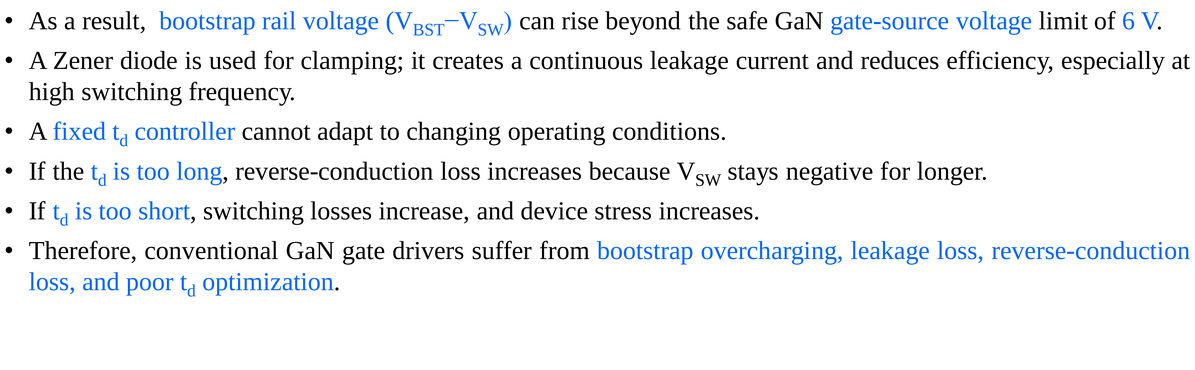


(a) (b) (c)

Fig 2. (a)Schematic of proposed GaN gate driver, (b) the t_d generator represents a dynamic t_d generator, and (c) is the t_d controller.

- The two GaN HEMTs, Q_H and Q_L, act as the high side and low side power switches.
- The dynamic t_d generator produces the switching signals V_H and V_L from the PWM input.
- The ZVS controller monitors the switching-node voltage (V_{SW}) and helps achieve zero-voltage switching.
- This reduces negative V_{SW}, prevents excessive charging of the C_{BST}, and improves switching efficiency.

Conventional GaN gate driver



(a) (b)

Fig. 1. (a) Schematic of a conventional GaN driver using C_{BST} = 20 nF, C_L= 10 µF, R_L =4.3 Ω. (b) Operational waveforms of the driver.

Main circuit blocks in Fig. 1(a)

- **Fixed t_{dead}** → : Generate deadtime (t_d) between V_H and V_L.
- **PWM** → Input pulse provided from the function generator.
- **Battery** →Supply input voltage (V_{IN}) and fixed drive voltage (V_{DRV}).
- **LS (Level shifter)** → levels up the voltage of V_H and V_L.
- **C_{BST} (Bootstrap capacitor)**→ : Provides gate drive voltage to Q_H.
- **Q_H and Q_L** → : High-side and low-side GaN switches.
- **D_Z** → : Zener diode used to ground the excessive current I_{DZ}.

Reverse Conduction loss (P_{RC})= $I_L \times t_{dead} \times V_{SD} \times f_{SW}$

Operational Waveforms of Proposed GaN gate driver

(a) (b) (c)

Fig 3. (a)Schematic of Comparator (CM_1),(b) Schematic of VCCR,(c) Operational waveforms of proposed GaN gate driver.

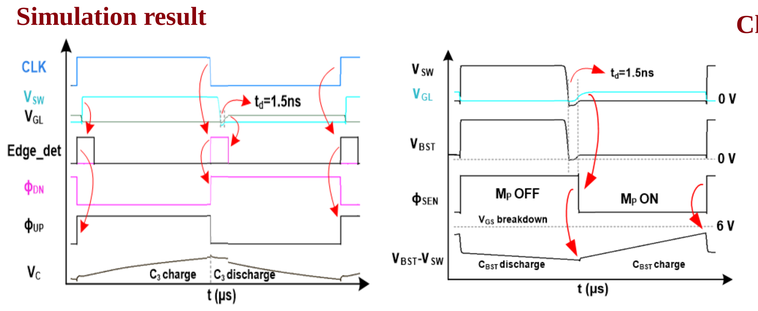
- The V_{SW} and V_{SNS} waveforms indicate that the switching-node voltage is monitored during the t_d interval.
- The Φ_{UP} charges the control node V_C, while Φ_{DN} discharges it.
- The changing V_C value determines the t_d dynamically, so the controller can shorten or extend t_d as needed.

Challenges in conventional GaN Gate driver

- Conventional GaN gate drivers use a bootstrap capacitor and Zener diode (D_Z) to drive the high-side switch.
- Due to No body diode in GaN, during t_d the switching node voltage (V_{SW}) can fall below ground. In this case, GaN conducts in the reverse direction.
- This negative V_{SW} causes excessive charging of the bootstrap capacitor (C_{BST}).
- As a result, bootstrap rail voltage (V_{BST}–V_{SW}) can rise beyond the safe GaN gate-source voltage limit of 6 V.
- A Zener diode is used for clamping; it creates a continuous leakage current and reduces efficiency, especially at high switching frequency.
- A fixed t_d controller cannot adapt to changing operating conditions.
- If the t_d is too long, reverse-conduction loss increases because V_{SW} stays negative for longer.
- If t_d is too short, switching losses increase, and device stress increases.
- Therefore, conventional GaN gate drivers suffer from bootstrap overcharging, leakage loss, reverse-conduction loss, and poor t_d optimization.

Simulation result and Chip fabrication

Simulation result

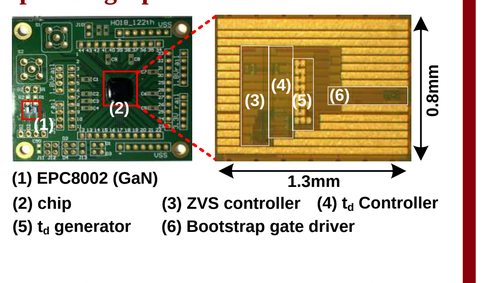


(a) (b)

Fig 4(a) and (b). Shows the simulation results of the proposed GaN gate driver.

- ✓ **Simulation results show that there is proper t_d between V_{SW} and V_{GL}.**
- ✓ **Simulation results match the operational waveforms in Fig. 3(c).**
- ✓ **A t_d of 1.5 ns is achieved.**
- ✓ **V_{IN}=12 V.**

Chip micrograph

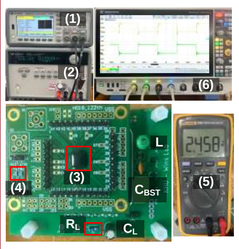


(1) EPC8002 (GaN)
(2) chip
(3) ZVS controller
(4) t_d Controller
(5) t_d generator
(6) Bootstrap gate driver

Fig 5. Chip micrograph of the GaN gate driver IC.

Results

Experiment setup



(1) CLK generator
(2) Power supply
(3) IC on test board
(4) EPC8002 (GaN)
(5) DMM
(6) Oscilloscpe

Fig. 6. Experiment setup.

- For experimental validation, a V_{IN}=12 V was applied.
- The converter achieved a V_{OUT}=2.5 V at light and heavy loads.
- The end-to-end efficiency of 89.4% is achieved.
- The measured output power was 2.08 W.

Experiment result

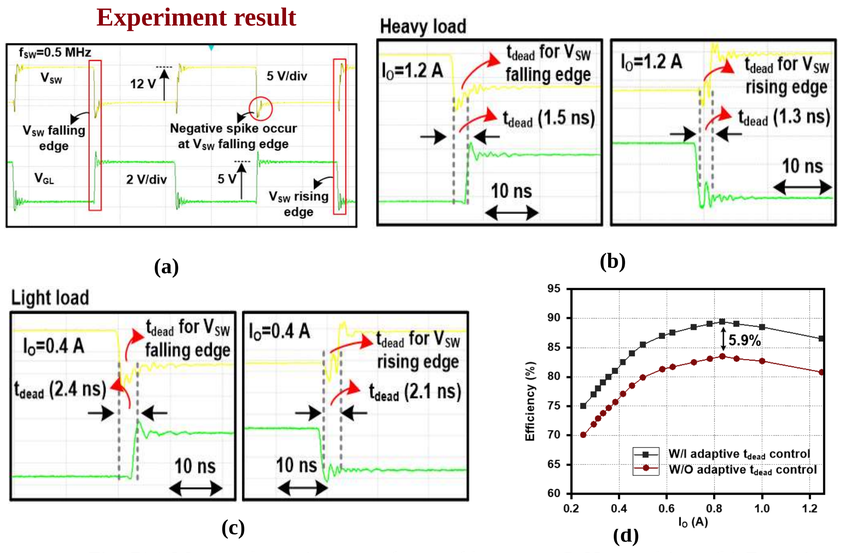


Fig. 7(a) Measured transient waveforms of bootstrap GaN gate driver, (b) Zoom-in view of V_{SW} trailing edge, (c) Zoom-in View of V_{SW} leading edge, (d) Measured efficiency with respect to load current.

Conclusion

Conclusion

- A GaN gate driver with active bootstrap and dynamic t_d control is proposed.
- The design prevents overcharging and reduces reverse-conduction loss.
- Fabricated in a 180 nm CMOS process, the driver demonstrates reliable operation at 12 V input, sub-3 ns t_d, and improved switching performance.
- Compared with the fixed t_d case, the proposed controller improves the peak efficiency by 5.9% and achieves 1.3 to 2.4 ns t_d operation.
- This work demonstrates a 12 V low-voltage PoL power-conversion prototype for automotive-related electronics; wider automotive input-range and higher-power validation will be considered as future work.

Acknowledgement

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